AMENDMENTS TO THE CLAIMS

The following is a complete listing of revised claims with a status identifier in parenthesis.

LISTING OF CLAIMS

1. (Original) A memory device, comprising:

a memory cell array;

an output buffer receiving data addressed from the memory cell array, and outputting the data based on a latency signal; and

a latency circuit selectively associating at least one transfer signal with at least one sampling signal based on CAS latency information to create a desired timing relationship between the associated sampling and transfer signals, storing read information in accordance with at least one of the sampling signals, and generating a latency signal based on the transfer signal associated with the sampling signal used in storing the read information.

2. (Original) The memory device of claim 1, wherein the latency circuit comprises:

a mapping unit selectively mapping a plurality of sampling signals to a plurality of transfer signals; and

a signal generator generating the latency signal based on the plurality of sampling signals mapped to the plurality of transfer signals.

3. (Original) The memory device of claim 1, wherein the latency circuit comprises:

a transfer signal generator generating a plurality of transfer signals based on a first signal; and

a sampling signal generator generating a plurality of sampling signals based on a second signal.

4. (Original) The memory device of claim 3, further comprising:

a first internal signal generator generating the first signal based on an external signal, the first signal having a same frequency as the external signal and offset from the external signal by a period of time to output the data from the output buffer.

5. (Original) The memory device of claim 4, further comprising:

a second internal signal generator generating the second signal based on the first signal, the second signal having a same frequency as the external signal and offset from the first signal by a period of time to output the data from the output buffer plus a period of time to generate the read information.

6. (Original) The memory device of claim 5, wherein

the transfer signal generator includes a first ring shift register clocked by the first signal, each position in the first ring shift register serving as one of the plurality of transfer signals; and

the sampling signal generator includes a second ring shift register clocked by the second signal, each position in the second ring shift register serving as one of the plurality of sampling signals.

7. (Original) The memory device of claim 6, wherein

the first signal is a data output clock signal; and further including,

an internal clock signal generator generating an internal clock signal based on the data output clock signal; and wherein

the second signal generator generates the second signal as a master clock signal based on the internal clock signal.

8. (Original) The memory device of claim 6, wherein the plurality of sampling signals and the plurality of transfer signals have a frequency substantially equal to a frequency of the external signal divided by a maximum number of CAS latency modes supported by the latency circuit.

9. (Original) The memory device of claim 5, wherein the second internal signal generator generates the second signal to have reduced jitter as compared to the first signal.

10. (Original) The memory device of claim 5, wherein the first internal signal generator generates the first signal using a delay locked loop circuit.

11. (Original) The memory device of claim 3, wherein the plurality of sampling signals and the plurality of transfer signals have a frequency substantially equal to a frequency of the external signal divided by a maximum number of CAS latency modes supported by the latency circuit.

12. (Original) The memory device of claim 1, wherein the latency circuit comprises:

a plurality of latches, each latch clocked by a respective sampling signal and latching the read information; and

a switch associated with each latch, each switch selectively outputting output from the associated latch based on a respective transfer signal.

13. (Original) The memory device of claim 12, wherein the latency circuit further comprises:

a latency latch latching output from the switches, and an output of the latency latch serving as the latency signal.

14. (Original) The memory device of claim 12, wherein a number of the latches equals a maximum number of CAS latency modes supported by the latency circuit.

15. (Original) The memory device of claim 1, wherein the latency circuit selectively associates at least one of the sampling signals with at least one of

the transfer signals by selectively activating at least one of a plurality of sampling signals.

16. (Original) The memory device of claim 15, wherein the latency circuit further comprises:

a sampling signal generator selectively generating a number of active sampling signals, the number being based on the CAS latency information.

17. (Original) The memory device of claim 16, wherein the sampling signal generator comprises:

a ring shifter clocked by a clock signal, each position in the ring shift register serving as a sampling signal; and

control logic cooperatively associated with the ring shifter and selectively activating at least one position of the ring shifter to selectively activate an associated sample signal based on the CAS latency information.

18. (Original) The memory device of claim 1, wherein the latency circuit selectively associates at least one of the transfer signals with at least one of the sampling signals by selectively activating at least one of a plurality of transfer signals.

19. (Original) The memory device of claim 18, wherein the latency circuit further comprises:

a transfer signal generator selectively generating a number of active transfer signals, the number being based on the CAS latency information.

20. (Original) The memory device of claim 19, wherein the transfer signal generator comprises:

a ring shifter clocked by a clock signal, each position in the ring shift register serving as a transfer signal; and

control logic cooperatively associated with the ring shifter and selectively activating at least one position of the ring shifter to selectively activate an associated transfer signal based on the CAS latency information.

21. (Original) The memory device of claim 1, wherein the latency circuit selectively associates at least one of the sampling signals with at least one of the transfer signals by selectively activating at least one of a plurality of sampling signals and at least one of a plurality of transfer signals.

22. (Original) The memory device of claim 21, wherein the latency circuit further comprises:

a sampling signal generator selectively generating a first number of active sampling signals, the first number being based on the CAS latency information; and

a transfer signal generator selectively generating a second number of active transfer signals, the second number being based on the CAS latency information.

23. (Original) The memory device of claim 22, wherein the first and second number are equal.

24. (Original) The memory device of claim 22, wherein

the transfer signal generator includes,

a first ring shifter clocked by a first signal, each position in the first ring shift register serving as a transfer signal, and

first control logic cooperatively associated with the first ring shifter and selectively activating at least one position of the first ring shifter to selectively activate an associated transfer signal based on the CAS latency information; and

the sampling signal generator includes,

a second ring shifter clocked by a second signal, each position in the second ring shift register serving as a sampling signal, and

second control logic cooperatively associated with the second ring shifter and selectively activating at least one position of the second ring shifter to selectively activate an associated sample signal based on the CAS latency information.

25. (Original) The memory device of claim 24, wherein

the first control logic controls a loop length of the first ring shifter; and

the second control logic controls a loop length of the second ring shifter.

26. (Currently Amended) The memory device of claim [[24]]22, wherein

the transfer signal generator includes,

a first ring shifter clocked by a first signal, and

first control logic cooperatively associated with the first ring shifter and selectively controlling a first number of stages in a first shift loop of the first ring shifter based on the CAS latency information, each stage included in the first shift loop generating an active transfer signal; and

the sampling signal generator includes,

a second ring shifter clocked by a second signal, and

second control logic cooperatively associated with the second ring shifter and selectively controlling a second number of stages in a second shift loop of the second ring shifter based on the CAS latency information, each stage included in the second shift loop generating an active sampling signal.

27. (Original) The memory device of claim 24, further comprising:

a first internal signal generator generating the first signal based on an external signal, the first signal having a same frequency as the external signal

and offset from the external signal by a period of time to output the data from the output buffer.

28. (Original) The memory device of claim 27, further comprising:

a second internal signal generator generating the second signal based on the first signal, the second signal having a same frequency as the external signal and offset from the first signal by a period of time to output the data from the output buffer plus a period of time to generate the read information.

29. (Original) A latency circuit, comprising:

a signal generator generating a latency signal based on a plurality of sampling signals and a plurality of transfer signals; and

a mapping unit mapping a plurality of reference signals to the signal generator as the plurality of sampling signals based on CAS latency information.

30-36. (Canceled)

37. (Original) A memory device, comprising:

a memory cell array;

an output buffer receiving data addressed from the memory cell array, and outputting the data based on a latency signal; and

a latency circuit selectively activating a first number of a plurality of sampling signals and a second number of a plurality of transfer signals based on CAS latency information to create a desired timing relationship between the first number of activated sampling signals and the second number of activated transfer signals, storing read information in accordance with at least one of the first number of activated sampling signals, and generating a latency signal based on an activated transfer signal associated with the activated sampling signal used in storing the read information.

38. (Canceled)

39. (Original) A method of controlling output of data from a memory device, comprising:

storing data for output in a buffer;

outputting the data from the buffer based on a latency signal; and

selectively activating a first number of a plurality of sampling signals and a second number of a plurality of transfer signals based on CAS latency information to create a desired timing relationship between the first number of activated sampling signals and the second number of activated transfer signals;

storing read information in accordance with at least one of the first number of activated sampling signals; and

generating a latency signal based on an activated transfer signal associated with the activated sampling signal used in storing the read information.